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ST Su, RZ Makki, T Nagle - Journal of Electronic **Testing**, 1995 - Springer
... **Transient Power Supply Current** Monitoring-A New **Test** Method for CMOS VLSI Circuits ... We use the **transient power supply current** as indicative of such switching. The iDDT **test** approach is not meant to com- pete or replace other **test** methods, but is meant to augment them. ...
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V Stopjaková, H Manhaeve, M ... - ... , automation and **test** in ..., 1999 - portal.acm.org
... due to the fact that these failures may prevent changes of the quiescent **power supply current** [5]-[6]. Therefore, the **transient power supply current testing** (I DDT **testing**) [7]- [8] can be conveniently used to augment the existing **test** methods and to enhance the defect coverage. ...
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G Gielen, Z Wang, W Sansen - Proceedings of the 1994 IEEE/ACM ..., 1994 - portal.acm.org
... all attempts of input signal selection, and a compu- tationally expensive **transient** circuit simulation ... A large number of circuits under **testing**, including both the fault-free and the ... Measurements are obtained from the simulated **power-supply current** followed by a discrete frequency ...
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JS Beasley, H Ramamurthy, J Ramirez-Angulo, M ... - **Test** Conference, 1993. . ., 1993
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GH Weiss, DE Young - Electrical Overstress/Electrostatic Discharge ..., 1995
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[PDF] **Power** distribution system design methodology and capacitor selection for modern CMOS technology si-list.net [PDF]
LD Smith, RE Anderson, DW Forehand, TJ ... - IEEE Transactions on ..., 1999 - si-list.net
... frequency of VRM and several bulk capacitors, b) time response of same PDS to **current transient**, c) 20 amp **current** transients at ... An HP4291 is used to measure capacitor ESR by soldering it to an SMA connector and attaching it to a **test** head through an APC-7 connector. ...
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... 1.0 Introduction **Transient** Signal Analysis (TSA) is a new parametric **testing** method for digital integrated circuits. In TSA, tran- sients in both the voltage waveforms at selected **test** points as well as **current** transients on the **power supply** are ana- lyzed to determine the presence ...
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... All CMOS circuits have a relatively large **transient current** associated with switching of the logic gates. ... I/O pins generally presents a noisier envi- ronment requiring a slower **test** rate. Tester **current** leakage presents a similar logic state dependent noise to the VDD pin of the IC. ...
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J Liu, RZ Makki, A Kayssi - Journal of Electronic **Testing**, 2000 - Springer
... use of the dy- namic **power supply current**, i DDT , for **testing** SRAMs ... Any time a cell switches states, a measurable dynamic **power supply current** is estab- lishedasaresultoftheinducedte mporarypathbetween ... switching of a cell will result in an unexpected **transient current** level in ...
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G Gielen, Z Wang, W Sansen - Proceedings of the 1994 IEEE/ACM ..., 1994 - portal.acm.org
... on the parameters of the kth type of faulty circuit, **transient** simulation and ... B. Bannister, "Can **supply** cur- rent monitoring be applied to the **testing** of analog as ... [3] D. Papakostas, A. Hatzopoulos, "Analogue **fault** identification based on **power supply current** spectrum," Electronics ...
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[PDF] Digital integrated circuit **testing** using **transient** signal analysis psu.edu [PDF]
J Plusquellic, D Chiarulli, S Levitan - International **Test** Conference, 1996 - Citeseer
... are based on the analysis of a circuit's paramet- ric properties, for example, propagation delay, magnitude of **supply current** or **transient** response ... for generating logic tests have been improved over time to handle more types of **fault** behaviors, parametric **testing** strategies offer ...
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[CITATION] A 2-ns detecting time, 2-µm CMOS built-in **current** sensingcircuit
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... Erroneous switching of a cell will result in an unexpected **transient current** level in the **power supply**. The detection of this unexpected level of **current** pulse can then be used to infer a defect. The i DDT **test** method was shown to detect all disturb **faults**, including read-destruct ...
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... Note that the defect-free responses in Figures 4 and 6 are different because a different **test pattern** was used in each case. ... in the FCMOS circuit also have a similar iDDT (recall that iDDT is directly com- puted from the **transient** portion of the AVDD waveform) **current** response. ...
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... It has also been addressed, in part, by attempting the detection of the **transient** (dynamic) component, /dd, of the **power supply current** using off-chip ... Application of the simple **test pattern** that is traditionally used to detect CSAFs will also yield, as a by-product, **fault** ...
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... A methodology for obtain- ing Selective IDD a **test patterns** was first proposed by Mat et al. [16]. ... All CMOS circuits have a relatively large **transient current** associated with switching of the logic gates. ... if the output pins are physically disconnected or tri-stated during the **test** and if ...
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CF Hawkins, JM Soden, AW Righter, FJ ... - International Test ..., 1994 - Citeseer
... IDDO (ZLs,sJ tests measure the quiescent V,, (YsJ **power supply current** of the IC [21]. ... The Z, ,, pseudo stuck-at-**fault** (PSAF) **test** applies a SAF **vector pattern** to the input nodes of each logic gate, but only propagates the signal to that gate's output node [42, 471. ...
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[PDF] **Test** challenges for deep sub-micron technologies psu.edu [PDF]
KT Cheng, S Dey, M Rodgers, K Roy - Design Automation Conference, 2000 - Citeseer
... This technique uses a Genetic Algorithm-based approach to generate **patterns** that maximize the ... IC's maximum operating frequency (Fmax) to establish a multi- parameter **test** technique for ... intrinsic and extrinsic (defect) leakages in IC's with high background stand-by **current**. ...
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IDDT testing versus IDDQ testing
Y Min, Z Li - Journal of Electronic Testing, 1998 - Springer
... where δ shows the variation times of average **transient current** between the **fault**-free and faulty circuits ... The IDDT **test** generation is to find a **test vector** pair to maximize the value of given by (6) for ... resolution limit, the **fault** is IDDT testable, and {v1,v2} is then the **test pattern** pair to ...
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T Dalstein, T Friedrich, B Kulicke, D Sobajic - IEEE Transactions on Power Delivery, 1996

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ST Su, RZ Makki, T Nagle - Journal of Electronic Testing, 1995 - Springer
... This requires, in part, the use of **fault** isolation circuitry for each pseudo-partition (see Section 4.2). ... This algorithm in- cludes the following two steps. Step 1. In this step the **test** vectors are gener- ated. ... Page 9. **Transient Power Supply Current** Monitoring 31 ...
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... 9;, Repeat fix different I types of faulty circuit Sampfing on the parameters of the kth type of faulty circuit, **transient** simulation and discrete frequency crans formation to obtain 9'(,). qpl,) ... 9, ... References [1] P. Nigh, W. Maly, "**Test** generation for **current** testing," IEEE ...
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... supply current of the IC [21]. **...** Many companies perform some form of I,,, testing, such as **power** down tests, with a small set of testpatterns (vectors **...** The Z, ,, pseudo stuck-at-**fault** (PSAF) **test** applies a SAF **vector pattern** to the input nodes of each logic gate, but only propagates the **...**
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... of the logic state of a memory cell results in a **transient current** pulse in the ... Keywords: Current-testable design, dynamic current monitors, dynamic **power supply** current, **fault** modeling, **pattern** sensitivity. ... there have been a number of studies aimed at reducing the **test** length [2]-[9 ...
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... All CMOS circuits have a relatively large **transient current** associated with switching of the logic gates. ... I/O pins generally presents a noisier envi- ronment requiring a slower **test** rate. ... One proposed design integrates the IDD Q monitor into the **power supply** in an attempt to reduce ...
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... Erroneous switching of a cell will result in an unexpected **transient current** level in the **power supply**. ... The i DDT **test** method was shown to detect all disturb **faults**, including read-destruct **faults** using a short **test** length of 5n where n is the number of cells, but this **test** method ...
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Y Min, Z Li - Journal of Electronic Testing, 1998 - Springer
... When some inputs change from logic 1(0) to logic 0(1), the **power supply** current ... where δ shows the variation times of average **transient current** between the **fault**-free and faulty circuits. ... hardware resolution limit, the **fault** is IDDT testable, and {v1,v2} is then the **test pattern** pair to ...
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... is typically on the order of tens of nanoamperes, while the **transient current** may reach ... Therefore, the average **power** dissipation overhead is about 12.4% due to the in ... Future work includes automatic **test** equipment interfacing, **test pattern** generation, and partitioning of large ...
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